Claim 1 previously canceled.

2. (Twice amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired, said first region directly adjacent said second region;

introducing a halogen-containing impurities into an exposed surface of said semiconductor substrate to form a higher halogen concentration in said first region than in said second region;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region; and

forming a first memory gate electrode on said second oxide layer thickness, said second oxide layer thickness formed on said semiconductor substrate in a memory region.

Please cancel claim 3.

4. (As previously amended) The method of claim 2 wherein introducing said halogen-containing impurities comprises an ion implantation.

5. (As previously amended) The method of claim 2 wherein introducing said halogen-containing impurities comprises introducing halogen-containing impurities into said first region and wherein said second region has substantially no halogen concentration therein.

6. (Twice amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region; and

wherein introducing said halogen-containing impurities comprises introducing halogen-containing impurities into said first region at a first concentration and introducing halogen-containing impurities into said second region at a second concentration, said first concentration greater than said second concentration, both said first and second concentrations having greater than 1 x 10^{14} carriers/cm^2.

7. (As previously amended) The method of claim 6 wherein introducing said halogen-containing impurities comprises an ion implantation.

8. (As previously amended) The method of claim 2 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

9. (As previously amended) The method of claim 2 wherein said semiconductor substrate also includes a third region where a third oxide layer thickness is desired, and wherein introducing said halogen-containing impurities also introduces halogen-containing impurities such that a different halogen concentration is formed in said third region than in said first region and in said second region.

10. (As previously amended herein) The method of claim 2 wherein said semiconductor device comprises a flash EEPROM semiconductor device.

11. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a floating gate electrode.

12. (As filed) The method of claim 11 wherein said first memory gate electrode is part of a stack gate cell.

13. (As filed) The method of claim 11 wherein said first memory gate electrode is part of a split gate cell.

14. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a control gate electrode.

15. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a stack gate cell.

16. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a split gate cell.

Claims 17-19 previously canceled.

20. (Twice amended herein) A method of forming a semiconductor integrated circuit, said method comprising:

providing a semiconductor substrate, said semiconductor substrate comprising a memory cell region, a first region for a MOS transistor, and a second region for a high voltage device;

forming a gate dielectric layer comprising an oxide overlying said semiconductor substrate including said first region and said second region;

selectively implanting halogen-containing impurities through said gate dielectric layer and into said second region, said halogen-containing impurities having a concentration greater than 1 x 10^{14} carriers/cm^2, said selectively implanting at an implant energy that is about 0.1 keV to about 40 keV; and

simultaneously forming a first thickness of dielectric material overlying said first region and forming a second thickness of dielectric material overlying said second region by an oxidizing process.

21. (Twice amended herein) The method of claim 20 **[A method of forming a semiconductor integrated circuit, said method comprising:**

providing a semiconductor substrate, said semiconductor substrate comprising a memory cell region, a first region for a MOS transistor, and a second region for a high voltage device;

forming a gate dielectric layer comprising an oxide overlying said semiconductor substrate including said first region and said second region;

selectively implanting halogen-containing impurities into said second region; and

simultaneously forming a first thickness of dielectric material overlying said first region and forming a second thickness of dielectric material overlying said second region by an oxidizing process;]

wherein said selectively implanting halogen-containing impurities into said first region also includes selectively implanting halogen-containing impurities into said second region such that said first region has a greater halogen concentration than said second region, said halogen concentration in said second region being greater than 1×10^{14} carriers/cm^2 and less than about 1×10^{15} carriers/cm^2.

22. (As filed) The method of claim 20 wherein said halogen containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

23 (As filed) The method of claim 20 further comprising forming a third thickness of dielectric material overlying a third region, said third region being spatially apart from said first region and said second region.

24. (As amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired, said first region directly adjacent said second region;

forming a dielectric layer on said substrate;

masking said dielectric layer to expose said first region;

introducing a halogen-containing impurities through said dielectric layer and into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region,

said oxidizing process comprising a thermal anneal at about 780 to about 1000 degrees Celsius, and for a duration of about ten (10) minutes to about five (5) hours.

25. (As previously added) The method of claim 24 wherein said introducing said halogen-containing impurities comprises an ion implantation.

26. (As previously added) The method of claim 24 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

27. (As amended herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired, a second region where a second oxide layer thickness is desired, and a third region where a third oxide layer thickness is desired;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region, and a different halogen concentration in said third region than in said first region and said second region, each of said higher halogen concentration and said different halogen concentration being in excess of 1×10^{14} carriers/cm^2; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region.

28. (As previously added) The method of claim 27 wherein said performing an oxidizing process also simultaneously forms said third oxide layer thickness at said third region.

Please add the following claims:

--29. The method of claim 6 wherein at least one of said first and second concentrations is greater than 1 x 10^{14} carriers/cm^2 and less than 1 x 10^{15} carriers/cm^2.

30. The method of claim 20 wherein said forming said first and second thicknesses of dielectric material comprises an anneal process performed at about 780 to about 1000 degrees Celsius, and for a duration of about ten (10) minutes to about five (5) hours.

31. The method of claim 30 wherein said anneal process is further performed at a pressure of about 760 Torr.--

REMARKS

Claims 2-16 and 20-28 have been examined. Claims 2, 6, 20, 21, 24 and 27 have been amended, claim 3 has been canceled and claims 29-31 have been added. Hence, claims 2, 4-16 and 20-31 are now pending. Reconsideration of the subject application as amended is respectfully requested.

The previously indicated allowability by the Examiner of claims 2-4, 6, 9, 11-16 and 21 has been withdrawn in view of the newly discovered reference to Grider et al., U. S. Pat. No. 6,093,659

Claims 2-9 and 20-28 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Grider et al.

Claim 10 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2-9 and 20-28.

Claims 11-16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2-9 and 20-28.